iATC
29C50 and 29C51
FEATURE CONTROL COMBO

PRELIMINARY

- **29C50 22-pin, 7 signaling channels**
- **29C51 28-pin, 10 signaling channels, secondary analog inputs and outputs**

- **External and User Programmable Transmit and Receive Gain**
- **Programmable Internal and External Hybrid Balance Network Select**
- **Programmable Analog, Digital, and Subscriber Loopback**
- **Programmable μ/A-Law Select**
- **Flexible Signaling Interface**
- **Secondary Analog Channel**
- **Three-Party Conferencing**
- **Low Power Consumption**

The Intel iATC 29C50/29C51 Feature Control Combo is an advanced user-probrammable, fully integrated PCM Codec with transmit/receive filters fabricated in a CMOS technology. This technology is built on CHMOS and will allow the 29C50 and 29C51 to realize the same excellent transmission performance as in the Intel 2913/2914 combo while achieving the low power consumption typical of CMOS circuits.

The 29C50/29C51 are the first members of Intel's third generation advanced telecommunication components. The Feature Control Combo supports the analog subscriber with a variety of added per-line features to the normal BORSCHT functions associated with the analog line circuit. Some of these features include secondary analog channels, programmable transmit and receive gain, on-chip or custom hybrid balancing network selection, a flexible signaling interface, and programmable μ or A-law conversions.

The 29C50/29C51 is intended for use with the 2952 Integrated Line Card Controller in digital switching environments. These components allow the system transmit and receive backplane highways to operate at different frequencies from that of the subscriber interface data channels. The 2952 handles the transfer of primary voice, secondary analog data, feature control, and signaling information between the backplane and up to 8 29C50/29C51's.

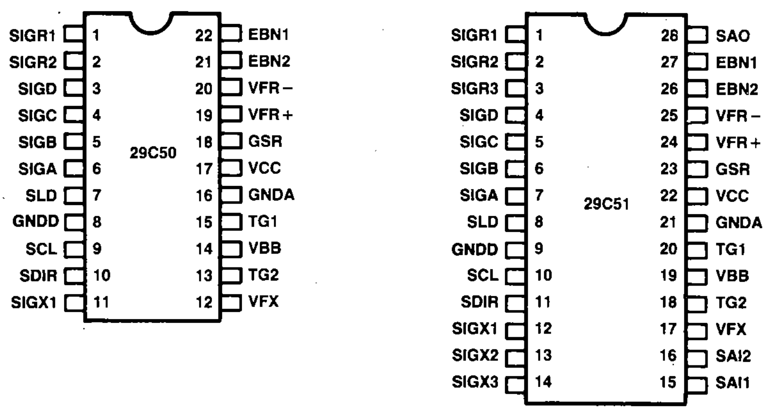


Figure 1. Pin Configuration

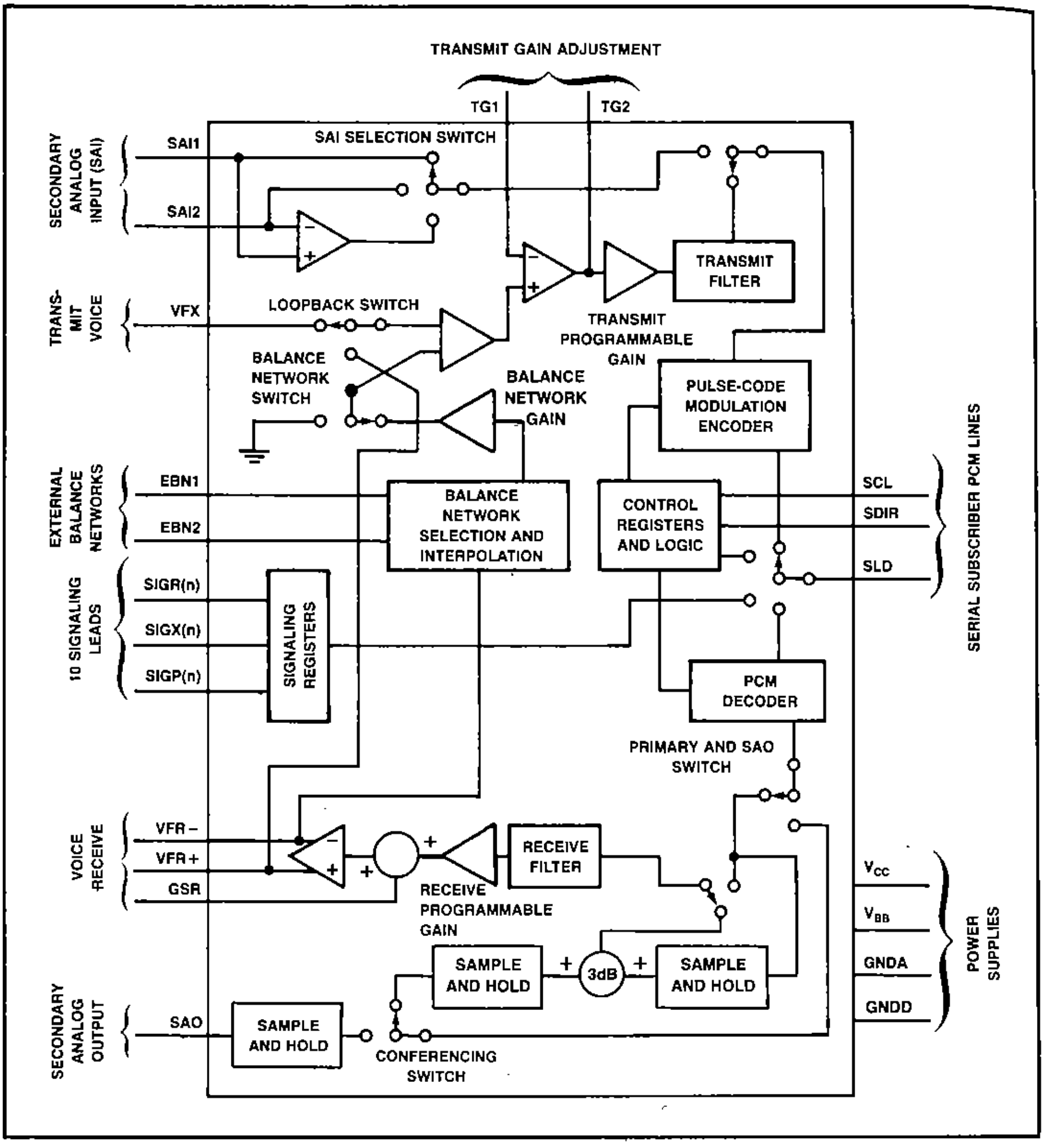


Figure 2. Block Diagram

Table 1. Pin Names

VFX	Analog Input	SCL	Subscriber Clock
VFR+, VFR−	Analog Output	SLD	Subscriber Data Link
SAI1, SAI2	Secondary Analog Inputs	SDIR	Subscriber Direction
SAO	Secondary Analog Output	TG1, TG2	Transmit Gain Adjust
GNDD	Digital Ground	GSR	Receive Gain Adjust
GNDA	Analog Ground	EBN1, EBN2	External Balance Network
V_{CC}	Power (+5V)	SIGX1, X2, X3	Transmit Signaling Input
V_{BB}	Power (−5V)	SIGR1, R2, R3	Receive Signaling Output
		SIGA, B, C, D	Programmable Transmit/ Receive Signaling Lead

Table 2. Pin Description

Symbol	Function
VCC	Most positive supply; input voltage is +5V±5%.
VBB	Most negative supply; input voltage is −5V±5%.
GNDA	Analog ground return line. Not internally connected to GNDD.
GNDD	Digital ground return line. Not internally connected to GNDA.
VFX	Analog voice input to transmit channel.
TG1	Inverting input to transmit gain adjusting op-amp. Feedback point for external gain adjusting resistor network up to 10k ohm.
TG2	Output of the transmit gain adjusting op-amp. Will drive external gain adjusting resistor network up to 10k ohm.
VFR+	Non-inverting output of the power amplifier. Capable of directly driving transformer hybrids or high impedance loads either single ended or differentially.
VFR−	Inverting output of power amplifier. Capable of directly driving transformer hybrids or high impedance loads either single ended or differentially.
GSR	Input to receive gain setting circuit. An external resistor network connected between VFR− and VFR+, and GSR sets the receive channel gain from 0dB to −9.54dB. Connecting GSR to GNDA will set the gain at −6.02dB.
EBN1	Input for the first external balance network.
EBN2	Input for the second external balance network.
SAI1	First secondary analog input, also the non-inverting input if differential secondary analog input mode is selected.
SAI2	Second secondary analog input, also the inverting input if differential secondary analog input mode is selected.

Symbol	Function
SAO	Secondary analog output, capable of driving loads of a least 10kΩ.
SCL	Subscriber clock. Supplied by the 2952 line card controller, this is a 512 kHz, 50% or 33% duty cycle clock. Input will accept TTL levels.
SDIR	Subscriber direction signal and frame sync. When high, SLD becomes an input and data is transferred from the 2952 to the 29C51. When low, the output buffer on the 29C51 SLD pin is enabled and data is transferred from the 29C51 to the 2952. Input will accept TTL levels.
SLD	Subscriber data link. A 512kbps bi-directional serial data port, which is clocked by SCL. SLD becomes a TTL compatible input when SDIR is high and an output capable of driving one TTL load when SDIR is low.
SIGX1 SIGX2 SIGX3	Transmit signaling inputs. Data present at SIGX(n) is latched by an internal signal preceding the falling edge of SDIR and is serially transferred on SLD during the transmit signaling byte. TTL compatible.
SIGR1 SIGR2 SIGR3	Receive signaling outputs. Data received serially on SLD during the receive signaling byte is latched on these outputs during the following byte. Capable of driving one TTL load.
SIGA SIGB SIGC SIGD	Programmable signaling pins. If the appropriate bit in the feature control memory is set high (either SIGDA, SIGDB, SIGDC, or SIGDD), the corresponding pin will become a receive signaling output, like SIGR(n). If the bit in the feature control memory is set low, the corresponding pin will become a transmit signaling input, like SIGX(n). Inputs will accept TTL level inputs, and outputs can drive one TTL load.

FUNCTIONAL DESCRIPTION

The 29C50/29C51 is a combined channel filter and PCM codec for use on analog line interface circuit boards in a digital telecommunications switching system. This device resides between the circuitry which provides the "BORSHT" functions for a given line, and the shared line board controller. It provides the transmit and receive voice-path filtering and companded analog-to-digital and digital-to-analog conversions necessary to interface a full duplex (4-wire) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system.

All features of the 22-lead device (29C50) are identical to that of the 28-lead device (29C51) except for the number of signaling pins and the secondary channel capabilities. There are 10 signaling channels available on the 29C51 configured as three transmit, three receive, and four programmable for either direction. Seven signaling leads are located on the 29C50 providing one transmit, two receive, and four programmable. There are no secondary analog inputs or outputs on the 29C50; however, three-party conferencing is still available.

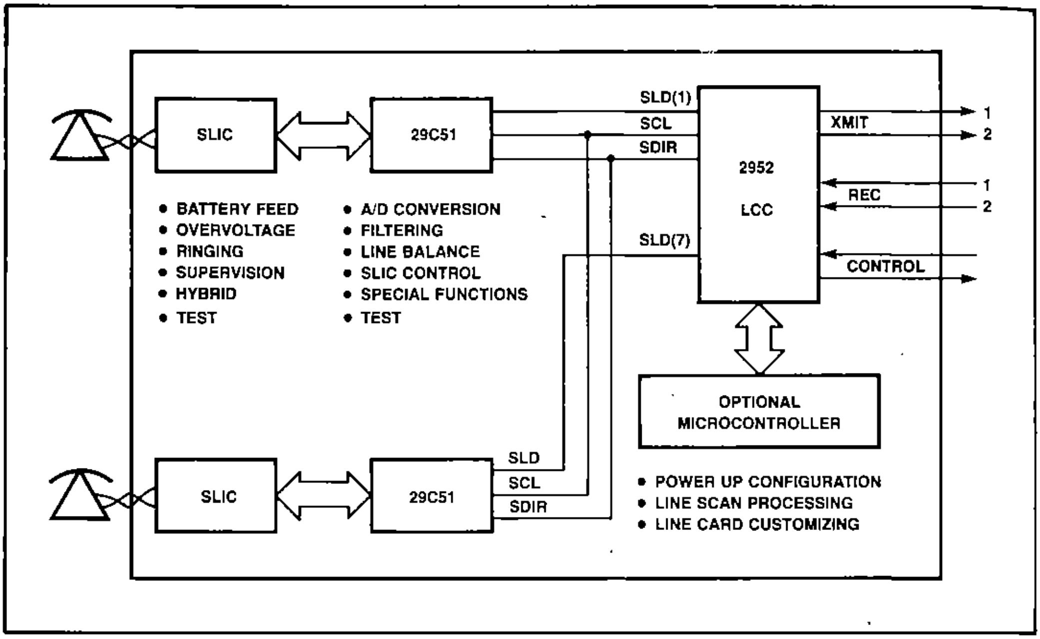


Figure 3. Analog Linecard

TRANSMIT AND RECEIVE OPERATION

Transmit Filter

A low pass anti-aliasing section is included on chip. This section typically provides 35dB attenuation at the sampling frequency. No external components are required to provide the necessary anti-aliasing function for the switched capacitor section of the transmit filter.

The passband section provides flatness and stopband attenuation which fulfills the AT&T D3/D4 specification and the CCITT G.712 recommendation. The 29C50 and 29C51 specifications meet the digital class 5 central office switching systems requirements. The transmit filter transfer characteristics and specifications will be within the limits shown in Figure 10.

A high pass section configuration rejects low frequency noise from 50 and 60 Hz power lines, 17 Hz European electric railroads, ringing frequencies and their harmonics, and other low frequency noise. Gain of up to 20dB can be set without degrading the performance of the filter.

Encoding

The output of the transmit filter is internally sampled by the encoder and held on an internal sample and hold capacitor. DC offset is corrected by an on-chip auto zero circuit. The signal is then encoded and presented as PCM data on the SLD lead on the first 8 bits of the XMIT half frame (fifth byte). Secondary analog input signals are routed directly to the encoder and output in the sixth byte on the SLD.

Decoding

The PCM words received on the SLD are demultiplexed and sent to the decoder. The decoded value is held on an internal sample and hold capacitor. If the secondary analog channel is being used, the PCM word received in the second byte on the SLD is decoded, then held on another sample and hold capacitor before appearing on the secondary analog output (SAO). If, however, conferencing has been selected, the two converted signals will be added and subsequently passed to the receive filter.

Receive Filter

The receive section of the filter provides a passband flatness and stopband rejection which fulfills the AT&T D3/D4 specification and the CCITT G.712 recommendation. The receive filter transfer characteristics and specifications will be within the limits shown in Figure 11.

GENERAL OPERATION

External Gain Setting

Both transmit and receive gain levels are factory trimmed, but can be modified by external resistors during line card assembly. The value of transmit gain is adjusted by connecting resistors RT1 and RT2 (see Figure 4) at the two external gain setting control pins, TG1 and TG2. These two pins are the input and output of an on-board gain amplifier stage, and the resistors provide the necessary input and feedback for gain control. The value of external gain is given by:

$$A = 1 + RT1/RT2$$

For unity gain, pins TG1 and TG2 are tied together. Similarly, for the receive section, external resistors RR1 and RR2 at pins VFR+, GSR, and VFR− set the external gain given by:

$$A = (RR1 + RR2)/(RR1 + 3RR2)$$

A value greater than 10k ohms and less than 100k ohms for R1+R2 is recommended. The output is capable of driving loads of 300 ohms at 3.2Vp single ended or 600 ohms at 6.4Vp differentially.

Three additional gain settings of 0dB, −6dB, and −9.54dB can be realized without using any external components by strapping pin GSR to VFR−, GNDA, and VFR+, respectively.

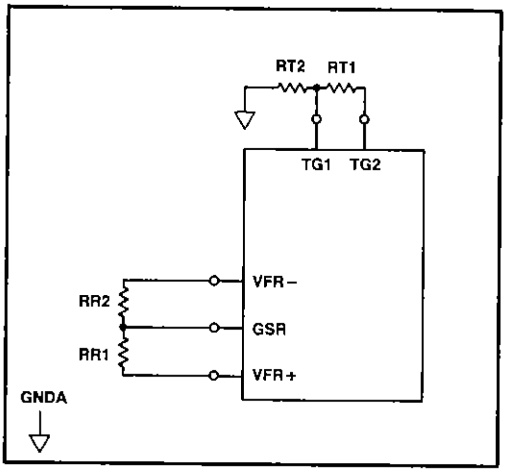


Figure 4. External Gain Connections

Hybrid Balancing Network

The 2- to 4-wire conversion necessary for subscriber interface is partially integrated on-chip. Network line balancing needed to minimize the trans-hybrid loss from the receive to transmit direction analog signals is handled internally. The three internal networks shown in Figure 6 may be selected by programming the appropriate feature control byte. These networks are integrated in a switched capacitor configuration and have single pole-zero characteristics in the 200 Hz to 3200 Hz range. They were chosen to serve a wide base of U.S. and European requirements, and can be used as standard line balancing networks or as test networks.

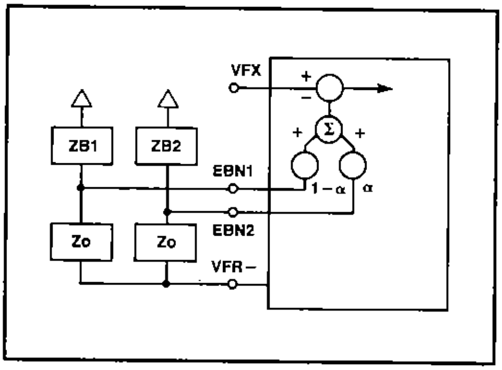


Figure 5. External Balance Network and Interpolation Configuration

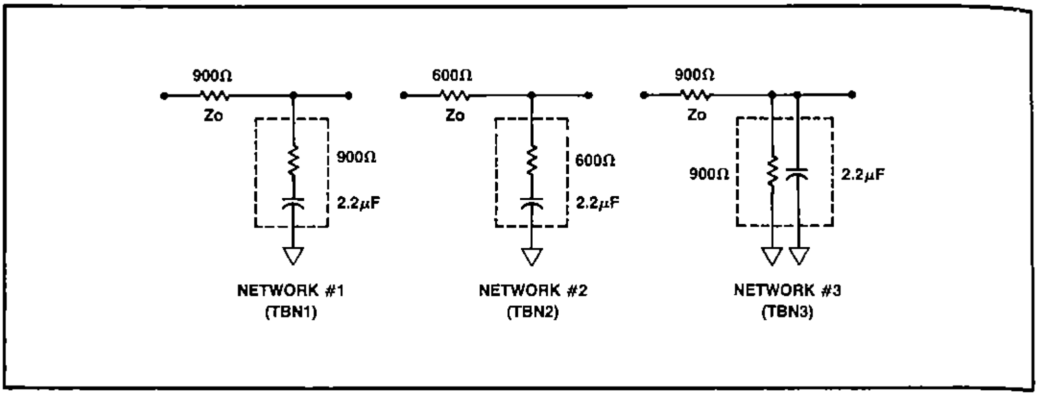


Figure 6. Internal Balance Networks

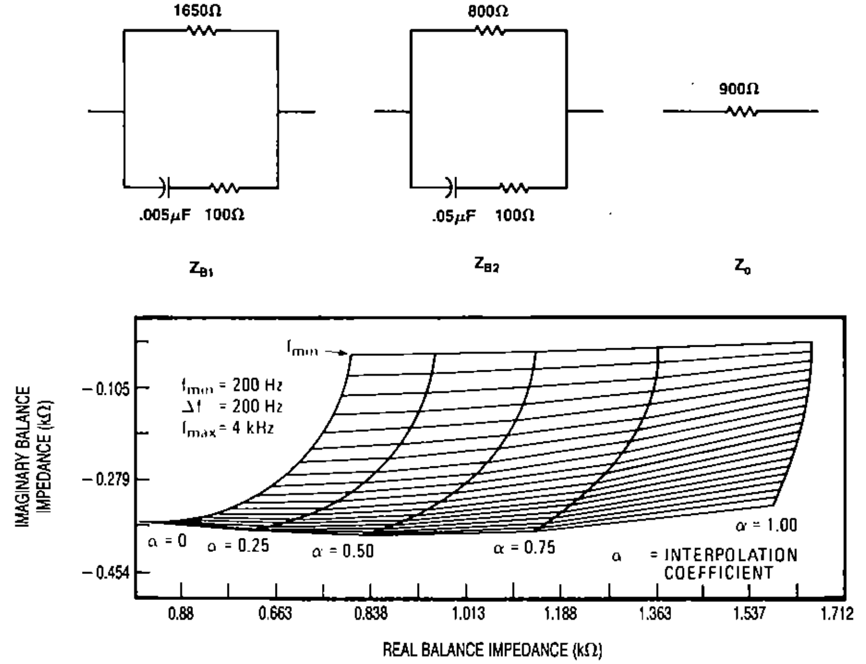


Figure 7. Typical External Balance Networks and Complex Impedance Plot

Additionally, the user may apply two external balance networks to accommodate varying subscriber loop characteristics (See Figure 5 for external connections). Presumably, these two networks can represent the two extremes of line conditions in different applications such as long or short loops and loaded or unloaded lines. To serve typical lines with characteristics in between the two extremes, the interpolation capability provides a weighted average of the network frequency characteristics. If the external network at EBN1 produces a transfer function H1(f) = ZB1 (Zo + ZB1) and the network at EBN2 produces H2(f) = ZB2 (Zo + ZB2), the balance signal can be programmed to have the transfer function H(f):

$$H(f) = \alpha\, H1(f) + (1 - \alpha)\, H2(f)$$

where "α" is the interpolation coefficient programmed to have any of the five values of 0, .25, .50, .75, or 1.0. Figure 5 displays how the subtraction of the coupling signal is implemented inside the device.

As an example, the two external networks shown in Figure 7 represent typical hybrid balance networks for loaded (ZB1) and unloaded (ZB2) analog loops. The graph in Figure 7 shows the real and imaginary components of the equivalent impedance of these two networks as a function of frequency and the interpolation coefficient.

Secondary Analog Channel/Conferencing

The 29C51 offers two simultaneous unfiltered information channels beyond the primary channel. Narrow band analog signals can be supplied for such applications as telemetry, teleconferencing, remote loop testing, or various control uses.

The secondary analog channel is accessed through two inputs, SAI1 and SAI2, sampled either single ended or differentially. The unfiltered secondary analog output, SAO, is a stair-step signal with the inherent sinx/x frequency rolloff following D/A conversion.

To allow three-party conferencing, the third party voice information can be transmitted and received during the data bytes carrying the secondary analog channel information. In the receive direction the primary and secondary voice signals are held on separate internal capacitors following D/A conversion, then passed through a −3dB attenuator and summed together. The combined signal is smoothed in the receive filter and passed onto the output power amplifier. In the transmit direction, the pulse-code modulation encoder inserts the primary voice into both the fifth and sixth SLD bytes.

Precision Voltage References

Voltage references are generated on-chip and are trimmed during the manufacturing process. Separate references are supplied for both the transmit and receive sections of the chip, each trimmed independently. These references determine the gain and dynamic range of the device and provide the user a significant margin for error in other board components.

SLD Interface

The 29C50 and 29C51 are intended for use with the 2952 Line Card Controller which manages the transfer of all voice, feature control and signaling data to and from the Feature Control Combo and the system backplane. The interface between the two consists of just three leads, two of which are clock signals and the third a unique serial bus for communication. Up to eight 29C50/29C51 feature control combos per line card can be controlled by one 2952, all sharing common clock signals, SCL and SDIR.

The subscriber direction (SDIR) lead provides an 8 kHz signal which divides each frame into transmit and receive halves. During the first half when SDIR is high (RCV half-cycle), data is transmitted from the 2952 to the 29C51 and in the second (XMIT half-cycle) transfer is from the 29C51 back to the 2952. Frame synchronization and all internal timing for the digital circuitry is derived from the rising edge of the SDIR signal.

The subscriber clock (SCL) input generated by the 2952 is a fixed 512 kHz clock signal allowing 64 bits (8 bytes) of data to be transferred on the SLD lead during each 125 μsec frame. Depending on 2952 master clock frequency, the SCL duty cycle can be either 50% or 33%.

The subscriber data link (SLD) is a bidirectional serial bus that transfers eight bytes of serial data to and from the 29C51 each frame. During the first half of each frame, RCV channel information is transferred to the 29C51 in four bytes consisting of primary voice, secondary analog, feature control, and signaling information. (The data byte actually contains the secondary analog channel information.) Similarly during the second half-cycle, four bytes of XMIT channel information are sent to the 2952. The MSB (bit 7) of each byte is sent first on the SLD. After the last valid signaling bit is transmitted to the 2952, the bus is placed in a high impedance state for at least one SCL clock cycle to prevent data contention on the bus. (See FCB#6 — Signaling Register.)

Upon power supply application and clocks SCL and SDIR applied, the 29C51 will automatically enter the power down state. During the transmit half cycle (29C51 talking to the 2952) a code of all ones will be sent to the controller during the VOX and DAX bytes.

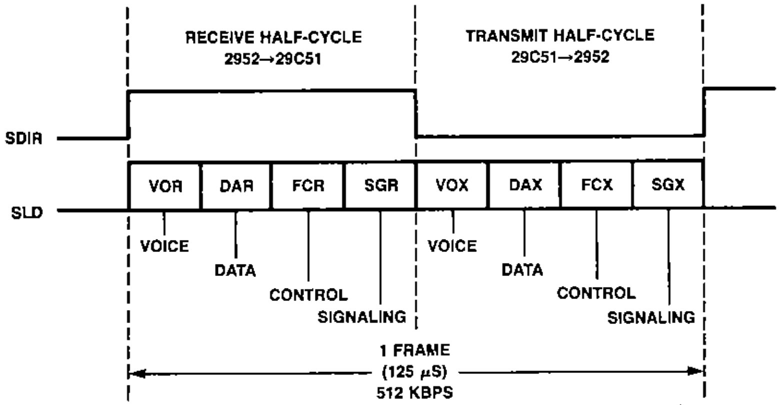


Figure 8. 29C51/2952 Interface

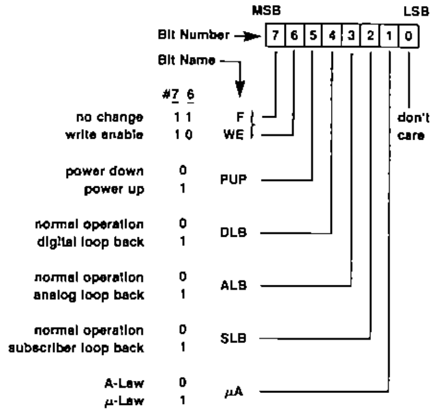
PROGRAMMABLE FEATURES

The 29C51 is configured by the 2952 line card controller by a set of six feature control bytes (FCB). These bytes of information are stored in internal registers which are serially multiplexed to and from the SLD interface in the third and seventh byte locations. The first two bits of each byte consist of a multiframe synchronization and write enable code. The framing bit (bit 7, MSB) establishes the beginning of a feature control frame when set to a logical zero, and increments the feature control counter when set to one. The second (bit 6) enables the writing to the 29C51 when it is the logical complement of the framing bit.

When writing new feature control information to the 29C51, the first byte should contain a framing (F) and write enable (WE) header of 01 (F=0 and WE=1). This designates a new frame of information to transfer. The subsequent bytes should each have F=1 to advance the counter, and WE=0 to enable the write operation.

The controller can also request to verify the feature control register contents by sending a 00 or 11 at the beginning of the byte to be read. To read the first byte, a 00 F/WE code should be sent while each subsequent byte should have a 11 header. An internal six-stage counter is set on the first byte verified then incremented once each 125μs frame. It is reset only upon detection of a 01 or 00 F/WE. Once the counter is greater than six, neither read nor write modes may be selected by sending the 29C51 a 11 framing and write enable code. The 29C51 will then echo in byte 7 the data it received in byte 3.

FCB #1 — Power Up/Down, Loop Back Mode, μ/A-Law Select Register



POWER UP AND DOWN

The 29C50/29C51 can be instructed to go into the power down or standby mode for reduced power consumption. In this mode, all analog inputs and outputs are placed in a high impedance state, inhibiting all primary voice and secondary data signals. A code of all ones will be output in the voice and data bytes on the SLD. Signaling and feature control information will continue to be processed to allow the 29C51 to be read or reprogramed, and to allow the backplane to monitor the subscriber line.

The 2952 can change the state of the feature control combo from standby to active by sending the first feature control byte only. All other register contents will be preserved during power down provided the power supplies remain connected.

LOOP BACK MODE SELECT

Three modes of remote testing are incorporated in the 29C50/51 and can be selected by appropriate coding in this register. The loopback features allow a number of tests to be performed to determine line quality and balancing. These include digital loop back, analog loop back, and subscriber loop back.

In the digital loopback mode, the combo retransmits the PCM words it receives in the voice and data bytes of the SLD back to the line card controller in the same frame. This feature allows path verification and testing of the circuit up to the slave device.

When the analog loopback mode is selected, the analog output VFR+ is internally connected to the analog input VFX. This feature allows functional testing of the combo as well as gain adjustment. The secondary analog channel is unaffected during this operation.

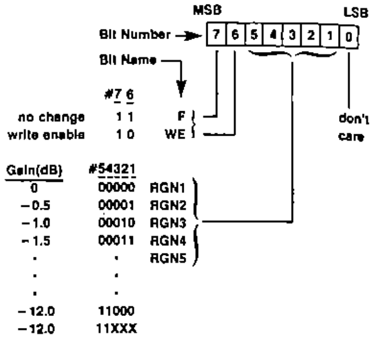
In the third test mode, subscriber loopback, the digital output of the A/D converter is internally connected to the input of the D/A converter. The analog signal input to VFX is sent through the transmit filter, encoded, then decoded, filtered and output to VFR+ and VFR−. This mode is used primarily for simplifying analog to analog testing from the subscriber side of the line card. If the secondary analog inputs and output are being used, they will be looped back in the same manner.

CONVERSION LAWS

The 29C50 and 29C51 can be selected for either μ-law or A-law operations. A user can select either conversion law by assigning the corresponding bit. A logical 1 in bit 1 would select μ-law while a logical 0 would select A-law conversions. Both conversions follow CCITT recommendation G.711.

FCB #2 — Receive Programmable Gain Register

The receive gain levels can be adjusted by applying external resistors as mentioned earlier, or by selective programming of this register. A range from 0 to −12dB in 0.5dB increments can be realized for the receive channel.

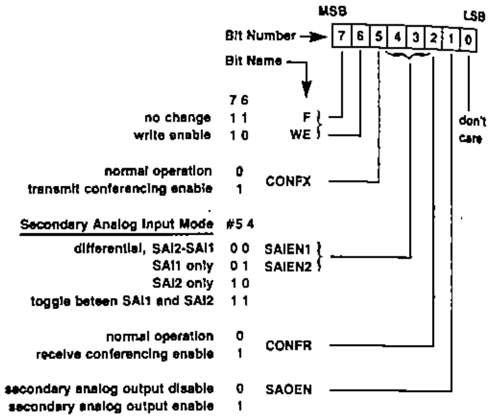


FCB #3 — Secondary Analog Channel Register

SECONDARY ANALOG INPUTS AND OUTPUTS

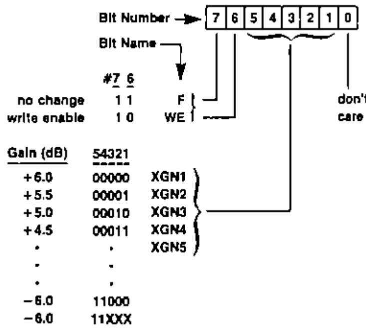
The two inputs to the secondary analog channel, SAI1 and SAI2, can be programmed to be encoded either single ended or differentially. An analog signal applied at the selected input may be encoded once every 125 μsec in addition to the primary voice channel. Alternatively, both SAI1 and SAI2 may be selected in which case each signal would be encoded in alternating frames at an effective sampling rate of 4 kHz. The LSB of the encoded word would toggle between 0 and 1 to designate which input it was encoded from. A "1" in the LSB represents SAI1 and a "0" for SAI2. The two inputs may also be used in a differential mode, resulting in SAI2 subtracted from SAI1.

The receive section of the secondary analog channel can be progammed to direct the data byte output onto SAO, or to add the analog signal to the primary voice channel for conferencing.



FCB #4 — Transmit Programmable Gain Register

The gain setting of the transmit section of the chip operates in the same manner as the receive gain register. A 12dB range from −6.0dB to +6.0dB in 0.5dB increments is available.



FCB #5 — Balance Network Select and Gain Register

BALANCE NETWORKS

The 29C51 offers a choice of internal or external hybrid balancing. Externally, two balance networks connected to pins EBN1 and EBN2 can be used independently, or as a weighted average of the two. The weighting factor, or interpolation coefficient, can range from 0 to 1 in steps of .25. Setting "α" to be 1 or 0 results in selecting either EBN1 or EBN2 respectively.

Three additional balance network configurations consisting of either a series or parallel RC circuit are located internal to the device. (See Figure 6).

GAIN SETTING

An additional 6dB gain in the balance signal path can be realized by coding this bit with a logical one. A logical zero provides unity gain.

MSB — LSB

Bit Number	Bit Name	Function	Code
7, 6	F / WE	no change	1 1
		write enable	1 0
5	BNE	disable balance network	0
		enable balance network	1
4, 3, 2	SBN1, SBN2, SBN3	INT TBN1	000
		INT TBN2	001
		INT TBN3	010
		EBN #1, α = 1	011
		EBN #2, α = 0	100
		α = .25	101
		α = .50	110
		α = .75	111
1	BNG	0dB gain (normal operation)	0
		6dB gain in signal path	1
0	don't care		

FCB #6 — Signaling Register

Four pins are provided on both the 29C50 and 29C51 chips to be used as selectable transmit or receive signaling inputs. A code of one in the respective bit commits the pin to receive signal information and a zero to transmit. The signaling field format as it appears on the SLD bus is shown in Figure 9 for both the 29C50 and 29C51. R1, R2, and R3 correspond to signaling information received on SIGR1, SIGR2, and SIGR3 respectively. Similarly, programmable pins SIGA, SIGB, SIGC, SIGD, and transmit pins SIGX1, SIGX2, SIGX3 are coded into the bit location as shown below.

MSB — LSB

Bit Number	Bit Name	Function	Code
7, 6	F / WE	no change	1 1
		write enable	1 0
5	L28	22 lead package	0
		28 lead package	1
4	SIGDA	SIGA is a transmit pin	0
		receive pin	1
3	SIGDB	SIGB is a transmit pin	0
		receive pin	1
2	SIGDC	SIGC is a transmit pin	0
		receive pin	1
1	SIGDD	SIGD is a transmit pin	0
		receive pin	1
0	don't care		

Receive Signaling SLD Byte #4

Bit (MSB→LSB)	7	6	5	4	3	2	1	0
29C51:	R1	R2	R3	A	B	C	D	—
29C50:	R1	R2	A	B	C	D	—	—

Transmit Signaling SLD Byte #8

Bit (MSB→LSB)	7	6	5	4	3	2	1	0
29C51:	X1	X2	X3	A	B	C	D	Z
29C50:	X1	A	B	C	D	Z	Z	Z

Z = High Impedance State
— = Don't Care State

Figure 9. Signaling Field Format

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .... −10°C to +80°C
Storage Temperature .... −65°C to +150°C
All Input and Output Voltages
with Respect to V_{BB} .... −0.3V to 13V
All Input and Output Voltages
with Respect to V_{CC} .... −13V to 0.3V
Power Dissipation 1.35W

**NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{BB} = −5v ±5%; SCL (50% duty), SDIR, SLD applied GNDD = 0v, GNDA = 0V.) Typical values are for T_A = 25°C and nominal power supply values

DIGITAL INTERFACE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{IL}	Input Leakage Current	−0.3		±10	μA	$V_{BB} \leq Vin \leq V_{CC}$
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.2		V_{CC} +.3	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} \geq -1.6$mA, 1 TTL load
V_{OH}	Output High Voltage	2.4			V	$I_{OH} \leq 50\mu$A, 1 TTL load

POWER DISSIPATION

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{CCL}	V_{cc} Operating Current		9		mA	
I_{BBL}	V_{BB} Operating Current		9		mA	
I_{CCO}	V_{cc} Standby Current		0.8		mA	
I_{BBO}	V_{BB} Standby Current		0.8		mA	
P_{D0}	Standby Power Dissipation		8		mW	
P_{DI}	Operating Power Dissipation		90		mW	

A.C. CHARACTERISTICS — TRANSMISSION PARAMETERS

(TG1 = TG2, Transmit Programmable Gain = 6dB; GSR = VFR−, Receive Programmable Gain = 0dB)

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
EmW	Encoder Milliwatt Response		±0.1		dB	Signal input of 0dBm0 f = 1.02KHz
DmW	Digital Milliwatt Response		±0.1		dB	f = 1.02KHz
$DmW_{\mu v}$	Digital Milliwatt Response VFR+, VFR−, μ-law		6.14		dBm	VFR + single-ended output R_L = 600Ω Receive input per CCITT G.711
DmW_{AV}	Digital Milliwatt Response VFR+, VFR−, A-law		6.17		dBm	
$DMW_{\mu s}$	Digital Milliwatt Response at SAO, μ-law		3.70		dBVrms	No load; no sin x/x correction
DmW_{AS}	Digital Milliwatt Response at SAO, A-law		3.73		dBVrms	No load; no sin x/x correction
$OTLP_X$	Zero Transmission Level Point Transmit Channel (0dBm0)		.788 .785		Vrms Vrms	A-law μ-law

GAIN TRACKING

Reference level = 0dBm0 for μ-law, −10 dBm0 A-law at 1.02KHz, TG1 = TG2, GSR = VFR−, Transmit Programmable Gain = 6dB, Receive Programmable Gain = 0dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
GT_T	Transmit Gain Tracking Error Sinusoidal Input; μ or A-law		±.25 ±.50 ±1.2		dB dB dB	+3 to −40dBm0 −40 to −50dBm0 −50 to −55dBm0
GT_R	Receive Gain Tracking Error Sinusoidal Input; μ or A-law		±.25 ±.50 ±1.2		dB dB dB	+3 to −40dBm0 −40 to −50dBm0 −50 to −55dBm0 AT&T PUB43801 and CCITT G.712 — Method 2

ANALOG INTERFACE, RECEIVE PRIMARY AND SECONDARY CHANNELS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
R_{OR}	Output Resistance, VFR+ VFR−		1		Ω	
V_{OSR1}	Output Offset, VFR+ or VFR−, single ended		50		mV	Relative to GNDA
V_{OSR2}	Output Offset, VFR+ to VFR−, Differential		75		mV	
C_{LR}	Load Capacitance, VFR+, VFR−			100	pF	
V_{OR1}	Max Output Voltage Swing across R_L, VFR+, VFR−, single-ended connection	±3.2			Vp	$R_L \geq 300\Omega$
V_{OR2}	Max Differential Output Voltage Swing, VFR+, VFR−	±6.4			Vp	$R_L \geq 600\Omega$
P_{OR}	Differential Output Power, VFR+, VFR−			15.3	dBm	$R_L = 600\Omega$
R_{ORS}	Output Resistance, SAO		25		Ω	
V_{OSR}	Output Offset, SAO		50		mV	
C_{LRS}	Load Capacitance, SAO			20	pF	
R_{LRS}	Load Resistance, SAO	10			KΩ	
V_{ORS}	Output Voltage Swing SAO	±3.2			Vp	$R_L \geq 10K\Omega$

ANALOG INTERFACE, TRANSMIT PRIMARY AND SECONDARY CHANNELS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
I_{BX}	Input Leakage Current, EBN1, EBN2, TG1		100		nA	−1.6V<VFX<1.6V
R_{IX1}	Input Resistance, VFX		500		KΩ	−1.6V<VFX<1.6V
R_{IX2}	Input Resistance, EBN1, EBN2, TG1		10		MΩ	−1.6V<VFX<1.6V
$CMRR_S$	Common Mode Rejection, SAI1, SAI2		40		dB	Differential SAI conversion
TGmax	Max Transmit Gain Adjust			20	dB	
V_{OTG}	Max Output Voltage Swing TG2	±1.6			v	$R_L \geq 10K\Omega$
C_{LX}	Load Capacitance, TG2			20	pF	
R_{LX}	Load Resistance, TG2	10			KΩ	

DISTORTION

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
SD_X, SD_R	Signal to Distortion, μ or A-law Sinusoidal input; CCITT G.712 — Method 2 Half Channel	35 29 25			dB dB dB	0 to −30dBm0 −30 to −40dBm0 −40 to −45dBm0
DP_X, DP_R	Single Frequency Distortion Products In Band (2nd or 3rd Harmonic Half Channel)		−50	−47	dB	Input = 1.02kHz 0dBm0 AT&T Advisory #64 (3.8)
IMD_1	Intermodulation Distortion, End to End Measurement			−40	dBm0	CCITT G.712(7.1)
IMD_2	Intermodulation Distortion, End to End Measurement			−50	dBm0	CCITT G.712(7.2)
SOS	Spurious Out of Band Signals, End to End Measurement			−27	dBm0	CCITT G.712(6.1)
SIS	Spurious In Band Signals, End to End Measurement			−40	dBm0	CCITT G.712(9)
D_{AX}	Transmit Absolute Delay		180		μs	0dBm0, 1.02kHz Includes delay through A/D
D_{DX}	Transmit Differential Envelope Delay; Relative to minimum envelope delay (1.4kHz)		170 95 45 105		μs μs μs μs	f = 500–600 Hz f = 600–1000 Hz f = 1000–2600 Hz f = 2600–2800 Hz
D_{AR}	Receive Absolute Delay		125		μs	0dBm0, 1.02kHz Includes delay through D/A
D_{DR}	Receive Differential Envelope Delay; Relative to minimum envelope delay (300 Hz)		45 35 85 110		μs μs μs μs	f = 500–600 Hz f = 600–1000 Hz f = 1000–2600 Hz f = 2600–2800 Hz

NOISE (Primary Channel)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
N_{XC1}	Transmit Noise, C-Message Weighted		12		dBrnCO	Transmit Gain Adjust = 0dB
N_{XP1}	Transmit Noise, Psophometrically Weighted		−78		dBm0p	Transmit Gain Adjust = 0dB
N_{RC1}	Receive Noise, C-Message Weighted		10		dBrnCO	Unity Gain; Idle Code
N_{RP1}	Receive Noise, Psophometrically Weighted		−80		dBm0p	Unity Gain; Idle Code
$PSRR_1$	V_{CC} Power Supply Rejection, Transmit Channel		−35		dB	Idle channel; 200mV P-P signal on supply DC to 50 KHz; Note 1.
$PSRR_2$	V_{BB} Power Supply Rejection Transmit Channel		−30		dB	Idle Channel; 200mV P-P signal on supply DC to 50 KHz; Note 1.
$PSRR_3$	V_{CC} Power Supply Rejection, Receive Channel		−35		dB	Idle channel, 200mV P-P signal on supply DC to 50 KHz; Note 1.
$PSRR_4$	V_{BB} Power Supply Rejection Receive Channel		−30		dB	Idle channel, 200mV P-P signal on supply DC to 50 KHz; Note 1.

CROSSTALK

Symbol	Parameter	Min	Type	Max	Units	Test Conditions
CT_{TR}	Crosstalk, Transmit Primary Voice to Receive Primary Voice		−75		dB	Input = 0dBm0, unity gain 1.02KHz; idle code on SLD voice and data bytes
CT_{RT}	Crosstalk, Receive Primary Voice to Transmit Primary Voice		−75		dB	0dBm0, 1.02 KHz signal at SLD receive voice byte; VFX = GNDA; secondary channels off
CT_{ST}	Crosstalk, Transmit Secondary Channels to Transmit Primary Voice		−70		dB	SAI = 0dBm0, 1.02 KHz; VFX = GNDA idle code on SLD voice and data bytes
CT_{SR}	Crosstalk, Receive Secondary Channel to Receive Primary Voice		−70		dB	0dBm0, 1.02 KHz at SLD data byte VFX = SAI = GNDA

NOTES:
1. Measured at SLD Voice bytes for transmit channel. Measured at $V_{FR}+$ for receive channel.

TRANSMIT VOICE FREQUENCY CHARACTERISTICS
TG1 = TG2, Transmit Programmable Gain = 6dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
G_{RX}	Gain Relative to Gain at 1.02kHz					0dBm0 Signal Input at VFX
	16.67Hz			−30	dB	
	50Hz			−25	dB	
	60Hz			−22	dB	
	200Hz	−1.8		−0.125	dB	
	300 to 3000Hz	−0.125		+0.125	dB	
	3300Hz	−0.35		+0.03	dB	
	3400Hz	−0.70		−0.10	dB	
	4000Hz			−14	dB	
	4600Hz and Above			−32	dB	
ΔG_{PX}	Programmable Gain Accuracy (Commulative Error)		±.25		dB	freq. = 1.02kHz for all steps

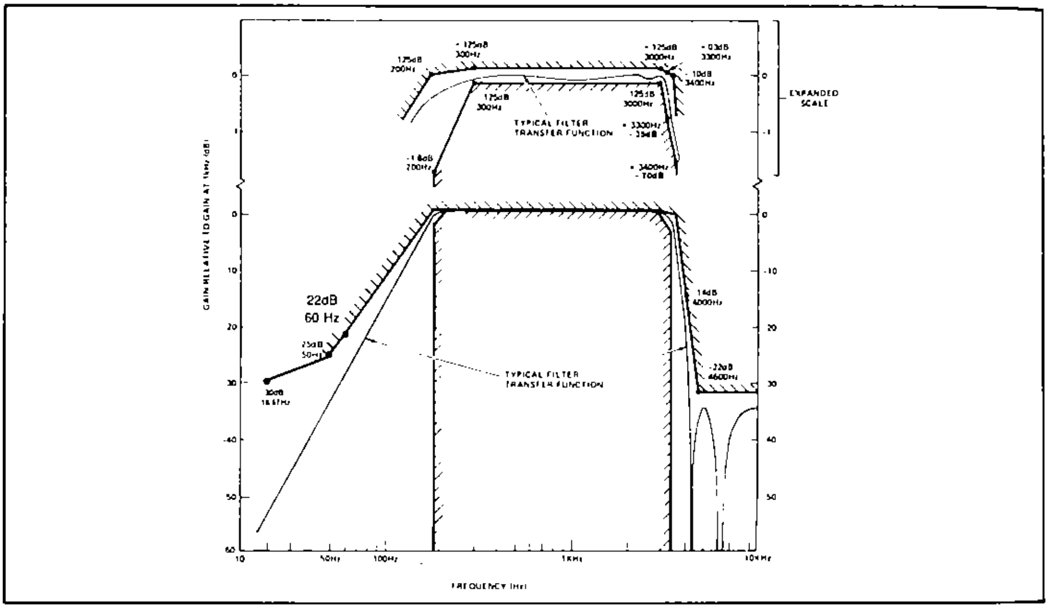
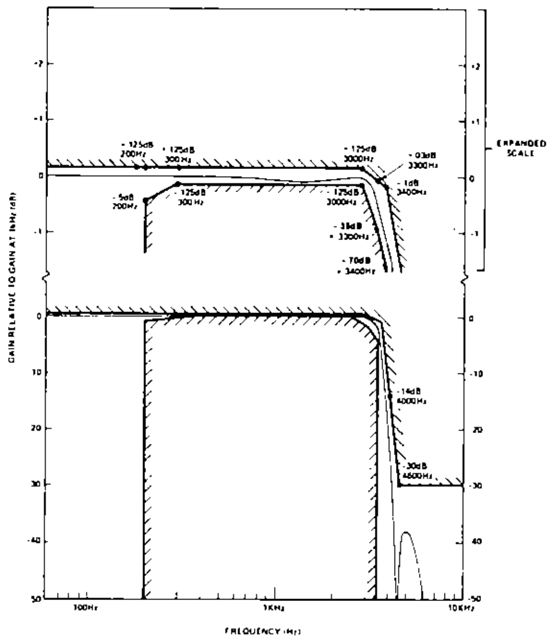


Figure 10. Transmit Voice Frequency Characteristics

RECEIVE FOICE FREQUENCY CHARACTERISTICS

GSR = VFR−, Receive Programmable Gain = 0dB

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
G_{RR}	Gain Relative to gain at 1.02kHz					0dBm0 input on SLD
	Below 200Hz			+0.125	dB	
	200Hz	−0.5		+0.125	dB	
	300 to 3000Hz	−0.125		+0.125	dB	
	3300Hz	−0.35		+0.03	dB	
	3400Hz	−0.70		−0.1	dB	
	4000Hz 4600Hz & Above			−14 −30	dB dB	
ΔG_{PR}	Programmable Gain Accuracy (Commulative Error		+.25		dB	f = 1.02kHz all steps



NOTES
1. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER AS A SEPARATE COMPONENT
2. TYPICAL TRANSFER FUNCTION OF THE RECEIVE FILTER DRIVEN BY THE SAMPLE AND HOLD OUTPUT OF THE INTEL 2910A AND 2911A CODECS. THE COMBINED FILTER/CODEC RESPONSE MEETS THE STATED SPECIFICATIONS.

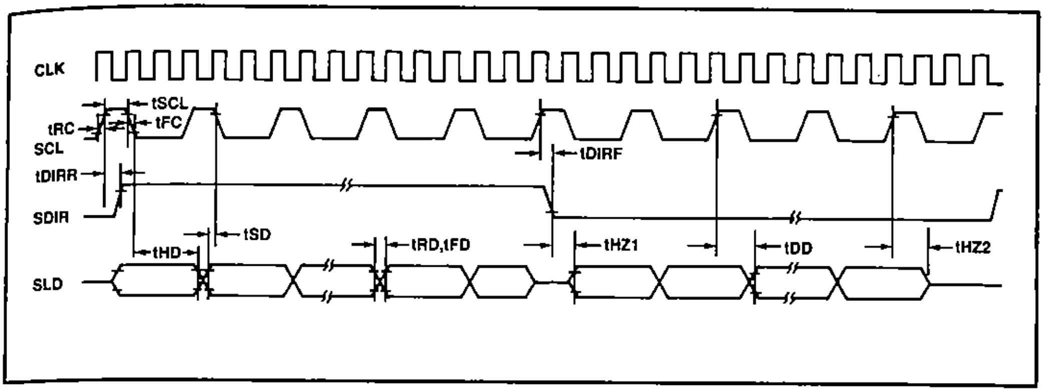
Figure 11. Receive Voice Frequency Characteristics

A.C. CHARACTERISTICS — TIMING PARAMETERS

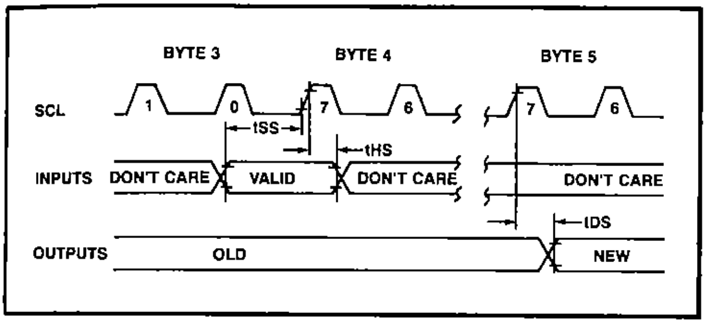
Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
T_{DC}	SCL Duty Cycle	28 45	33 50	38 55	% %	2952 CLK Clock = 1.544 or 1.536MHz 2952 CLK CLock ≥ 2.048MHz
t_{RC} T_{FC}	Rise, Fall Times, SCL			50	ns	
T_{RD} T_{FD}	Rise, Fall Times, SLD			50	ns	
T_{DIRR}	SCL to SDIR Delay	−100		100	ns	
T_{DIRF}	SCL to SDIR Delay	−100		+420	ns	
T_{DD}	SCL to SLD Delay	0		200	ns	29C51 Transmitting*
T_{SD}	Set-up Time, SLD to SCL	100			ns	2952 Transmitting
T_{HD}	Hold Time, SCL to SLD	100			ns	
T_{HZI}	SDIR to SLD Active	0		100	ns	Byte 1, Bit 1 29C51 Transmitting
T_{HZ2}	SCL to SLD High Impedence	0		100	ns	After last SIGX bit
T_{SS}	Set-up time, signaling inputs to SLD Byte #4, Bit 7	1			μs	
T_{HS}	Hold time, SLD Byte 4 Bit 7 for all signaling inputs	1			μs	
T_{DS}	Delay SLD Byte 5 to signaling outputs			1	μs	

*In cases where the T_{DIF} is positive, T_{DD} is to be measured from the SDIR edge.

TIMING PARAMETERS (CLK = 1.544 MHz, 33% duty cycle)



SIGNALING TIMING



A.C. TESTING INPUT, OUTPUT WAVEFORM

INPUT/OUTPUT

A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" and 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".